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APPLICATION FOR LETTERS PATENT

FOR

AN ARRANGEMENT FOR ESD PROTECTION OF AN INTEGRATED CIRCUIT

This application claims priority to Swedish Application No. 0102960-2 filed on September 6, 2001

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An Arrangement For ESD Protection Of An Integrated Circuit

Cross Reference to Related Application

[0001] This application is a continuation of copending International Application No. PCT/SE02/01535 filed August 28, 2002 which designates the United States, and claims priority to Swedish application no. 0102960-2 filed September 6, 2001.

Technical Field of the Invention

[0002] The present invention relates generally to integrated circuits and more specifically to electrostatic discharge protection of integrated circuits.

Background Of The Invention

[0003] Electrostatic discharges (ESDs) may, as is well known, damage electronic devices, particularly electronic semiconductor devices fabricated on conducting, semiconducting, insulating or semiinsulating substrates, such as integrated circuits.

[0004] Devices for ESD protection are conventionally incorporated in input/output paths of most semiconductor devices in order to shunt excessive charge away from the sensitive circuits.

[0005] In input paths of semiconductor devices, often some protection against high input currents is provided, such as an electrical resistance connected in the input path, this resistance limiting the input current. This resistance is conventionally located outside the bonding pad.

[0006] For high frequency applications at GHz frequencies, however, a resistance creates several problems. The RxC product of the resistance and the input capacitance of the circuit sets the limit of the highest operation frequency.

Furthermore, the resistance itself creates noise, which is deleterious in low noise applications.

Summary Of The Invention

[0007] The object of the invention is to provide a device for protecting a high frequency integrated circuit against excessive positive and/or negative voltages, such as ESDs, without having to add extra processing steps when fabricating the integrated circuit.

[0008] This is attained in accordance with the invention by an arrangement for protecting a high-frequency integrated circuit against higher voltages than normal operating voltages on an input/output terminal connected to a bonding pad in that the arrangement comprises a semiconductor varistor that is produced between the bonding pad and the input/output terminal of an integrated circuit in one and the same process on one and the same die and that has low essentially constant resistance for said normal operating voltages and higher resistance for said higher voltages.

Brief Description Of The Drawing

[0009] The invention will be described more in detail below with reference to the appended drawing on which

[0010] **Fig. 1** illustrates an embodiment of an arrangement according to the invention for protecting an input amplifier of an integrated circuit against ESDs by means of a varistor,

[0011] **Fig. 2** is a resistance versus voltage diagram of the varistor in Fig. 1,

[0012] **Fig. 3** illustrates a first embodiment of a varistor to be used in Fig. 1, and

[0013] **Fig. 4** illustrates a second embodiment of a varistor to be used in Fig. 1.

Description Of The Invention

[0014] In accordance with the invention, a silicon integrated varistor is used as a current limiting component in an arrangement for ESD protection of a silicon integrated circuit for high frequency applications.

[0015] It should be pointed out that varistors can be designed in a number of ways for this purpose, where different physical phenomena can be utilized. The simplest way to achieve the desired effect is to use the fact that the velocity of electric carriers, i.e. electrons and holes, saturates with increasing strength of an electric field. It follows that the current through the varistor saturates even if the voltage across the varistor continues to increase.

[0016] Fig. 1 illustrates an embodiment of an arrangement according to the invention for protecting an input amplifier 1 of an integrated circuit (not further shown) against ESDs appearing on an input terminal of the amplifier 1 that is connected to a bonding pad 2.

[0017] In accordance with the invention, a varistor 3 is integrated between the input terminal of the amplifier 1 and the bonding pad 2 in order to limit any appearing ESD current.

[0018] In a manner known per se in connection with ESD current limiting high-resistance resistors, the interconnection point between the varistor 3 and the bonding pad 2 is connected to a so-called primary current shunting device.

[0019] In the embodiment shown in Fig. 1, the primary current shunting device comprises a diode 4 that is connected with its anode to the interconnection point between the varistor 3 and the bonding pad 2 and with its cathode to a positive voltage V_A, and a diode 5 that is connected with its cathode to the interconnection point between the varistor 3 and the bonding pad 2 and with its anode to ground GND.

[0020] The interconnection point between the varistor 3 and the input terminal of the amplifier 1 can be connected to a so-called secondary current shunting device that, however, also can be omitted.

[0021] In the embodiment shown in Fig. 1, the secondary current shunting device comprises a diode 6 that is connected with its anode to the interconnection point between the varistor 3 and the amplifier 1 and with its cathode to the positive voltage V_A, and a diode 7 that is connected with its cathode to the interconnection point between the varistor 3 and the amplifier 1 and with its anode to ground GND.

[0022] The primary and secondary current shunting devices shunt any appearing ESD current to V_A or ground GND.

[0023] It is to be understood that other current shunting devices can be utilized, e.g. thyristor diodes.

[0024] In accordance with the invention, the varistor 3 is designed to have low and essentially constant resistance within a range of normal operating voltages of the amplifier 1 and higher resistance for higher voltages than the normal operating voltages.

[0025] An exemplary resistance R versus voltage V diagram of the varistor 3 is shown in Fig. 2. As indicated in the diagram in Fig. 2, the resistance R of the varistor is supposed to be low and essentially constant for operating voltages between V0 and VI.

[0026] Fig. 3 shows a first embodiment of the varistor 3 in Fig. 1 that can be used for ESD protection in accordance with the invention.

[0027] The embodiment of the varistor in Fig. 3 has been produced in a P-substrate 8, e.g. comprising boron, into which an N- well 9, e.g. comprising phosphorous, has been diffused from the top of the substrate 8. Two N+ regions 10, 11

have been implanted into the N- well 9 from the top of the substrate 8. The N+ regions 10, 11 are separated by an isolator 12 that extends into the N- well 9. Isolators 13, 14 that also extend into the N- well 9 are provided on the other side of the respective N+ region 10 and 11. The isolators 12, 13 and 14 comprise e.g. field oxide or shallow trench isolation.

[0028] To connect the varistor in Fig. 3 to the amplifier 1 and the bonding pad 2 as illustrated in Fig. 1, contacts 15 and 16 are provided on top of the respective N+ region 10 and 11. The contacts 15, 16 comprise e.g. $TiSi_2$ or $CoSi_2$. The bottom side of the substrate 8 is normally grounded.

[0029] For normal operating voltages V0-V1 of the amplifier 1 in Fig. 1, the resistance is low and essentially constant between the contacts 15 and 16 of the varistor in Fig. 3 as illustrated by the diagram in Fig. 2. Current will flow from the N+ region 10 via the N- region 9 to the N+ region 11.

[0030] When the potential difference between the contacts 15 and 16 of the varistor in Fig. 3 increases above the normal operating voltages of the amplifier 1 in Fig. 1 such as when an ESD appears, i.e. when the electric field between the N+ regions 10 and 11 increases above the normal electric field between the N+ regions 10 and 11, the velocity of electric carriers, in this case electrons, between the N+ regions 10 and 11 will become saturated. Thus, the current through the varistor in Fig. 3 will become saturated even if the electric field continues to increase. In other words, the resistance will increase with increasing voltage across the varistor in Fig. 3, i.e. voltages>V1, as illustrated by the diagram in Fig. 2.

[0031] The doping level of the N- well 9 and the dimensions of the isolator 12 are chosen such as to fulfil the electrical characteristics in the diagram in Fig. 2. If not carefully chosen, the described device will behave as a resistor or will have characteristics that are unsuitable for a protective device.

[0032] Fig. 4 shows a second embodiment of the varistor 3 in Fig. 1 that can be used for ESD protection in accordance with the invention.

[0033] The embodiment of the varistor in Fig. 4 has been produced in a P-substrate 17, e.g. comprising boron, into which an N- well 18, e.g. comprising phosphorous, has been diffused from the top of the substrate 17. Three separate N+ regions 19, 20 and 21 have been implanted into the N- well 18 from the top of the substrate 17 between two isolators 22, 23 that extend into the N- well. The isolators 22, 23 comprise e.g. field oxide or shallow trench isolation.

[0034] Contacts 24, 25 and 26 are provided on top of the respective N+ region 19, 20 and 21. The contacts 24, 25 and 26 comprise e.g. $TiSi_2$ or $CoSi_2$. The bottom side of the substrate 17 is normally grounded.

[0035] The contacts 24 and 26 that are located next to the isolators 22 and 23 of the varistor in Fig. 4 are to be connected to the amplifier 1 and the bonding pad 2 as illustrated in Fig. 1.

[0036] Isolating layers 27, 28, e.g. comprising SiO_2, are provided between the contacts 24, 25 and 25, 26, respectively. Gates 29, 30, e.g. of polysilicon, are provided on top of these isolating layers 27, 28. These gates 29, 30 are interconnected with the contact 25 on top of the N+ region 20.

[0037] For normal operating voltages of the amplifier 1 in Fig. 1, the resistance is constant between the contacts 24 and 26 of the varistor in Fig. 4 as illustrated by the diagram in Fig. 2. Current will flow from N+ region 19 to N+ region 20 and from N+ region 20 to N+ region 21.

[0038] In case of a positive ESD voltage appearing on e.g. contact 24, the potential of the contact 24 will be higher than the potential of the contact 25, i.e. of the gates 29 and 30.

[0039] This causes the N- region under the gate 29 to become depleted of electrons starting from the contact 24. Hereby, the resistance between the N+ regions 19 and 20 will increase. However, in the N- region under the gate 30, electrons will accumulate.

[0040] Besides the resistance increase caused by the depletion of electrons under the gate 29, the velocity of electric carriers, in this case electrons, between the N+ regions in the varistor in Fig. 4 will become saturated when the electric field between the N+ regions increases above the normal electric field between the N+ regions. Thus, the current through the varistor in Fig. 4 will also become saturated even if the electric field continues to increase. In other words, the resistance will increase with increasing voltage across the varistor in Fig. 4 as illustrated by the diagram in Fig. 2.

[0041] It should be obvious to anyone skilled in the art that similar types of varistors such as varistors based on JFETs or MESFETs or combinations thereof (also combinations with the varistors described above) can be used for ESD protection in accordance with the invention.